# GSV2001

1 In to 2 Out HDMI2.0 Repeater with Audio Extraction/Insertion

September, 2019

# PRODUCT SPECIFICATION

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# Glossary

| Term | Definition |
|---|---|
| DDC | Display Data Channel |
| EDID | Extended Display Identification Data |
| ESD | Electrostatic Discharge |
| HDCP | High-bandwidth Digital Content Protection |
| HDMI | High-Definition Multimedia Interface |
| HPD | Hot Plug Detect |
| $I^2C$ | Inter-Integrated Circuit |
| $I^2S$ | Integrated Interchip Sound |
| MCU | Microcontroller Unit |
| MISO | Master In Slave Out |
| MOSI | Master Out Slave In |
| OTP | One Time Programmable |
| PCM | Pulse Code Modulation |
| S/PDIF | Sony/Philips Digital Interface Format |
| SPI | Serial Peripheral Interface |
| TMDS | Transition Minimized Differential Signaling |
| SCDC | Status and Control Data Channel |
| CEC | Consumer Electronics Control |
| CSC | Color Space Conversion |

# 1 General Information

## 1.1 General Information

The GSV2001 is HDMI1.4/2.0 compatible, HDCP 1.4/2.2 supported, configurable 1-in-2-out repeater device. All 2 outputs are identical on transmitter capability.

The HDMI input and output maximum processing pixel clock frequency is 600MHz which means the video resolution can support up to 4kx2k@60Hz 4:4:4 8-bit. The maximum processing audio sample frequency is 192K Hz for non-compression timing. GSV2001 supports HDR10 and Dolby Vision HDR as input and output.

For audio insertion and extraction, the versatile TTL pin bus of GSV2001 can be configured as either input mode or output mode regarding platform requirement. GSV2001 can support up to 8-channel I2S or 2-channel S/PDIF, 3D and multi-stream audio. In TDM mode, each audio pin supports up to 8 channels.

Internal Scaler and Color Space Converter enables the input and output to be timing format independent and capable of long distance transmission.

With powerful HDMI Rx equalizer and Tx pre-emphasis capability, GSV2001 can cascade itself (or GSV2000 series chips) with at least 7 stages for all HDMI 1.3/1.4/2.0 timings.

An internal Clock Generator can be used to generate 4 independent output clocks, which will greatly remove complexity of using dedicated clock device.

## 1.2 Features

### 1.2.1 HDMI Video Input and Output

- Compliant with HDMI2.0b, HDMI1.4b
- Compliant with HDCP2.2/2.3 and HDCP1.4
- Data rate up to 18Gbps
- Programmable HDMI Tx output swing, slew-rate, pre-emphasis
- Adaptive receiver equalization
- AC-coupling capable
- Color Space Converter supports any conversion between different color spaces
- HDR supported (HDR10/HDR12/Dolby Vision/HLG)
- 5V tolerance on DDC/HPD/CEC
- Arbitrary video stream matrix between HDMI Rx and HDMI Tx

### 1.2.2 Audio Input/Output

- SPDIF/I2S/HBR/DSD/TDM Audio Extraction
- SPDIF/I2S/HBR/DSD/TDM Audio Insertion
- Configurable direction for each Audio bus
- Arbitrary audio stream matrix between HDMI Rx/HDMI Tx/Audio bus

### 1.2.3 Internal Downscaler

Scaler is only used to downscale 4k UHD timings to 2k FHD timings. The horizontal resolution and vertical resolution are both cut in half while frame rate remains the same.

### 1.2.4 Color Space Converter

Color Space Converter can convert RGB and YCbCr by the following table. It should be noted that YCbCr 422 shares the same color space with YCbCr 444 in internal routing. So any conversion that YCbCr 444 supports, YCbCr 422 also supports it.

Table 1. Color Space Converter Support Table

| From | To | To |
|---|---|---|
| **RGB** | YCbCr 444 | YCbCr 420 |
| **YCbCr 444** | YCbCr 420 | RGB |
| **YCbCr420** | YCbCr444 | RGB |

### 1.2.5 Clock Generator

Internal Clock Generator has 4 independent clock outputs ranging 25MHz~600MHz. Clock Generator generates output clocks based on divider/multiplier ratio of GSV2001's 27MHz oscillator. The no-compensation PLL circuit architecture minimizes output clock jitter. With fast PLL acquisition time, clock generator output clock frequency matches its ratio register settings in nano-seconds.

### 1.2.6 CEC

There is an internal CEC engine for handling CEC low level transactions. Customer design only needs to manipulate I2C registers for reading and writing CEC commands.

## 1.3 Chip Application Modes

### 1.3.1 Audio Extraction and Video Distribution

GSV2001 has 1 HDMI input port and 2 HDMI output ports. All of the ports are HDCP 1.4 and HDCP 2.2 capable.

One important purpose of extracting HDMI encrypted stream is to extract audio, process it in audio signal processing chip (DSP/FPGA e.g.). As shown below, TTL audio pins can be configured as output to implement this feature. It should be noted that extracted audio stream is routed from the selected HDMI input to distribute to HDMI outputs.

Limited by the only audio TTL bus, when audio extraction is implemented, audio insertion can not be implemented. So when using audio extraction, both Txs' audio can only be streamed from HDMI Rx rather than from external audio input.

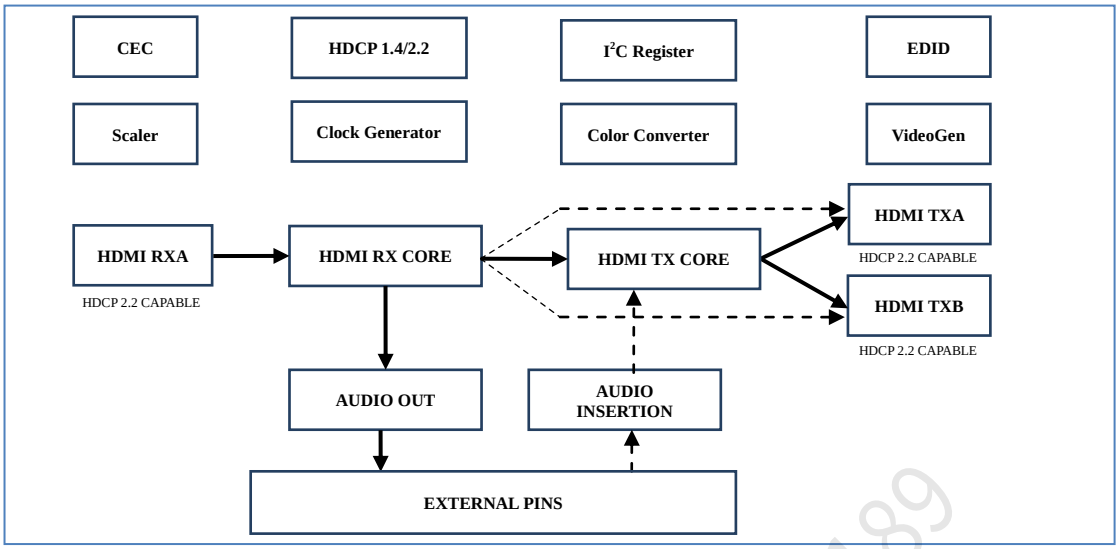



Figure 1. GSV2001 audio extraction diagram

## 1.3.2 Audio Insertion and Video Distribution

Inserted audio can be routed to any individual Tx or both Tx streams while HDMI video is still routed from HDMI Rx.

Limited by the only audio bus, when audio insertion is implemented, audio extraction can not be implemented. In this mode, both Txs' audio can be streamed either from HDMI Rx or external audio input.

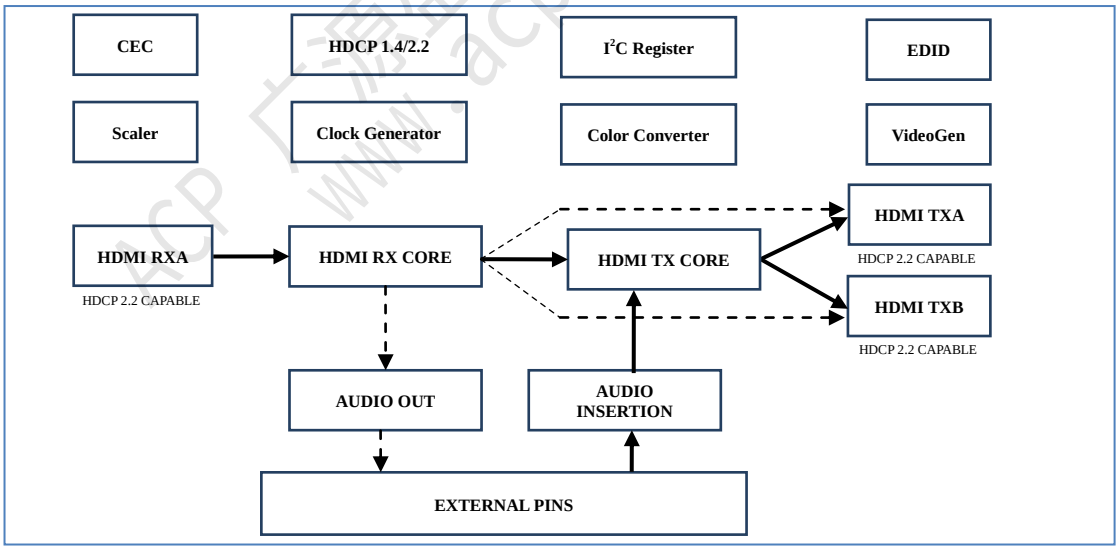



Figure 2. GSV2001 audio insertion diagram

## 1.3.3 HDMI 2.0 to HDMI 1.4 downscaler

GSV2001 has a built-in scaler and color converter. These blocks enable the chip to do internal video processing for matching HDMI source and sink's capability with a wider range and better performance. Flexible connection between IPs creates versatile

usage modes.

Here is an example of 4K YCbCr 420 (300MHz pixel clock) input, 4K YCbCr 420 (300MHz pixel clock) output and 1080p YCbCr 422 (150MHz pixel clock) output. It should be noted that Tx Core can still do color space conversion (except for YCbCr420) without Color Conversion block. This makes HDMI output flexible in color space.

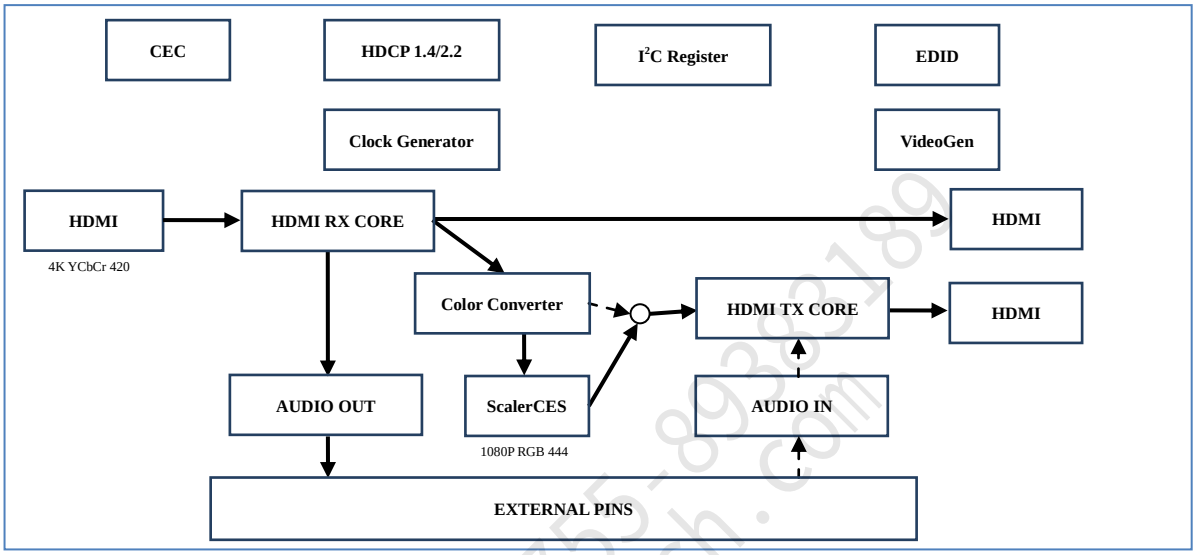



Figure 3. GSV2001 4K 420-to-1080p 422 diagram

## 1.3.4 HDMI 2.0 YCbCr 420 color space conversion

Here is an example of 4K RGB 444 (600MHz pixel clock) input, 4K YCbCr 422 (600MHz pixel clock) output and 4K YCbCr 420 (300MHz pixel clock) output. It should be noted that Tx Core can still do color space conversion (except for YCbCr420) without Color Conversion block. This makes HDMI output flexible in color space.

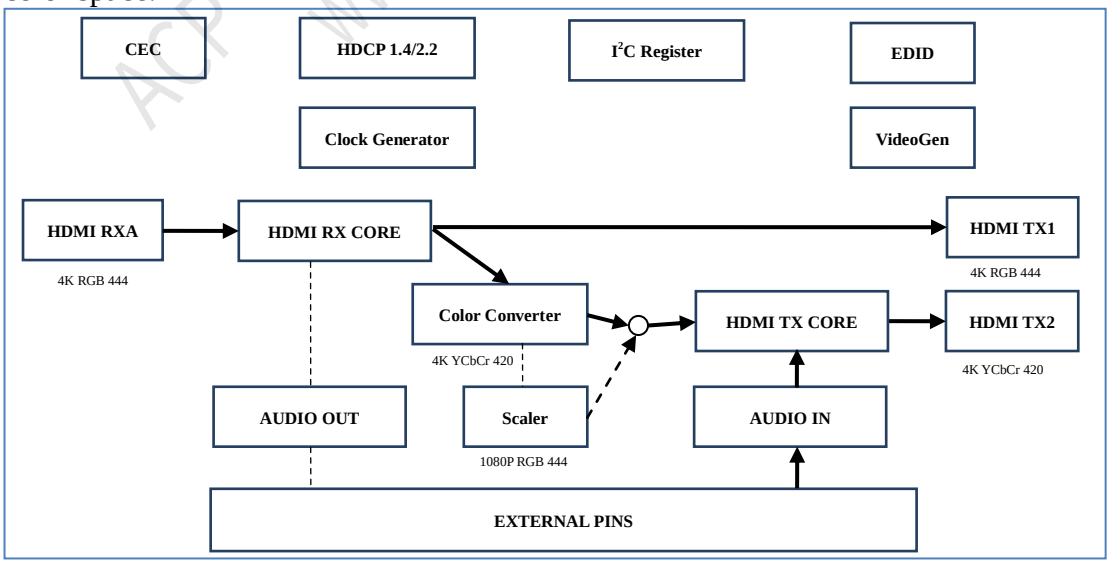



Figure 4. GSV2001 4K 444-to-4K 420 diagram

### 1.3.5 Enabling Clock Generator

When using Clock Generator to generate clock outputs, TxB's 4 differential pairs are occupied. The pins are internally pulled up to 3.3V with maximum 20mA differential current. Each PLL output clock has its independent ratio register setting.

4 pairs of GSV2001 differential output clock are recommended to be AC-coupled when connecting to device's differential clock input. If DC-coupled, GSV2001's differential output clock is internally pulled-up to 3.3V. In single-end clock application, each 50% duty-cycle differential clock output pair can be separated to clocks with 180 degrees phase shift.

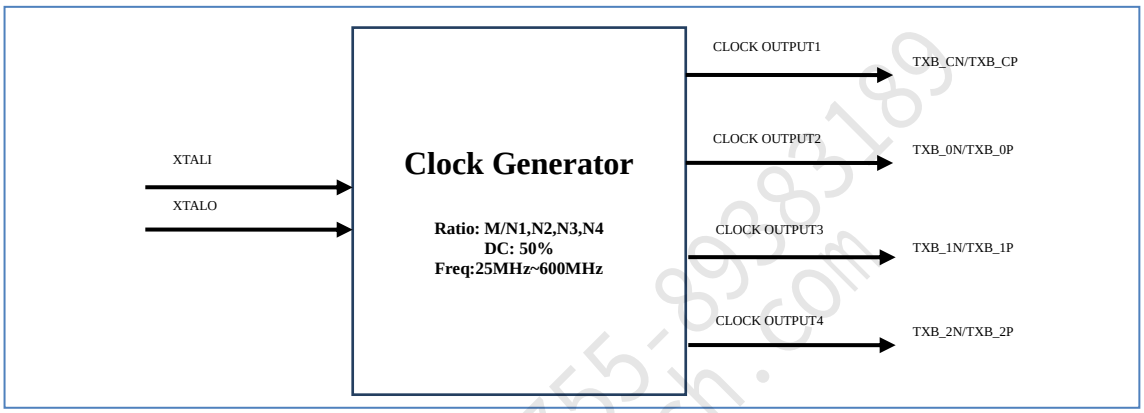



Figure 5. GSV2001 Clock Generator diagram

## 1.4 Audio Bus Output Capability

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. Normal Pin Setting is as below.

Table 2. I2S/SPDIF Audio Extraction

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AP0 | SDATA[0] | Output | I2S Data, default stereo channels |
| AP1 | SDATA[1] | Output | I2S Data, 3/4 channels |
| AP2 | SDATA[2] | Output | I2S Data, 5/6 channels |
| AP3 | SDATA[3] | Output | I2S Data, 7/8 channels |
| AP4 | SPDIF | Output | SPDIF channel |
| AP5 | LRCLK/WS | Output | Fs (0 = Left, 1 = Right) |
| SCLK | BCLK | Output | Fixed to 64Fs |
| MCLK | Sys Clock | Output | Selected from 128Fs/256Fs/384Fs/512Fs |

For HBR application, SPDIF are also capable of sending out with 4 pins.

Table 3. HBR Audio Extraction in SPDIF

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AP0 | SPDIF[0] | Output | SPDIF Data[0], 1/2 channels |
| AP1 | SPDIF[1] | Output | SPDIF Data[1], 3/4 channels |
| AP2 | SPDIF[2] | Output | SPDIF Data[2], 5/6 channels |

| | | | |
|---|---|---|---|
| AP3 | SPDIF[3] | Output | SPDIF Data[3], 7/8 channels |
| AP4 | SPDIF | Output | SPDIF channel, 1/2 channels |

## 1.5 Audio Bus Input Capability

When Audio Bus is set to Input, either I2S or SPDIF can be selected as audio input source. It should be noted that MCLK must be externally fed into GSV chip in I2S audio insertion mode.

For SPDIF input, GSV series chip can detect Sampling Frequency and automatically update it in Channel Status with GSV software. For I2S input, software designer needs to indicate the current input sampling frequency in software.
Common application modes are listed.

Table 4. Stereo I2S Input

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AP0 | SDATA[0] | Input | I2S Data, default stereo channels |
| AP5 | LRCLK/WS | Input | Fs (0 = Left, 1 = Right) |
| SCLK | BCLK | Input | Fixed to 64Fs |
| MCLK | Sys Clock | Input | Selected from 128Fs/256Fs/384Fs/512Fs |

Table 5. SPDIF Input

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AP0 | SPDIF | Input | SPDIF channel |

Table 6. 8 channel I2S Input

| Pin Name | Alias | Direction | Description |
|---|---|---|---|
| AP0 | SDATA[0] | Input | I2S Data, default stereo channels |
| AP1 | SDATA[1] | Input | I2S Data, 2/3 channels |
| AP2 | SDATA[2] | Input | I2S Data, 4/5 channels |
| AP3 | SDATA[3] | Input | I2S Data, 6/7 channels |
| AP5 | LRCLK/WS | Input | Fs (0 = Left, 1 = Right) |
| SCLK | BCLK | Input | Fixed to 64Fs |
| MCLK | Sys Clock | Input | Selected from 128Fs/256Fs/384Fs/512Fs |

# 2 Pin Description

## 2.1 Pin Diagram

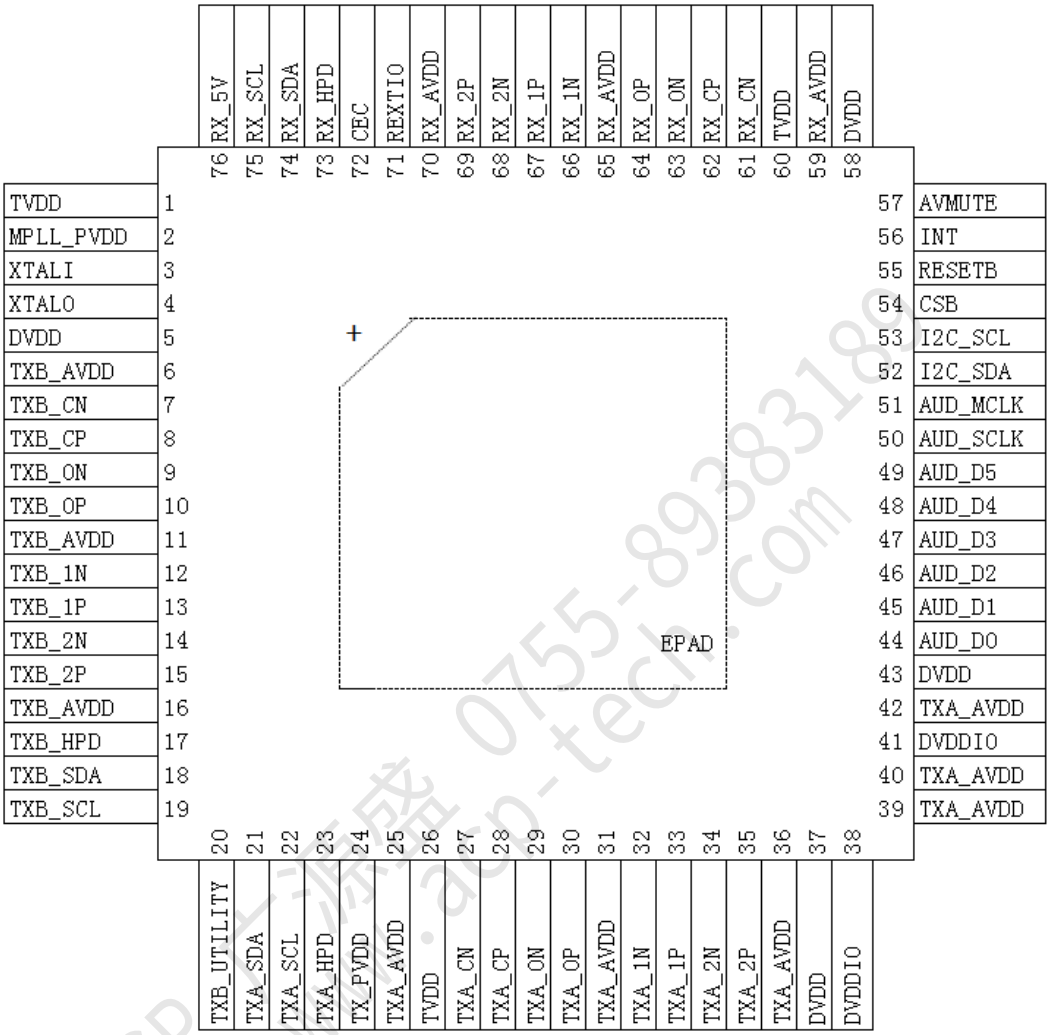



Figure 6. Pin Mapping

## 2.2 Pin Description

Table 7. Pin Description

| Pin No. | Pin Name | Direction | Description |
|---|---|---|---|
| 1 | TVDD | Power | Analog 3.3V voltage power supply |
| 2 | MPLL_PVDD | Power | 1.2V voltage power supply for MPLL |
| 3 | XTALI | I/O | 27M Crystal Input |
| 4 | XTALO | I/O | 27M Crystal output |
| 5 | DVDD | Power | Digital 1.2V voltage power supply |
| 6 | TXB_AVDD | Power | Analog 1.2V voltage power supply for TXB Port |
| 7 | TXB_CN | I/O | TXB Negative TMDS clock output |
| 8 | TXB_CP | I/O | TXB Positive TMDS clock output |
| 9 | TXB_0N | O | TXB Negative TMDS differential line driver data output [0] |
| 10 | TXB_0P | O | TXB Positive TMDS differential line driver data output [0] |
| 11 | TXB_AVDD | Power | Analog 1.2V voltage power supply for TXB Port |
| 12 | TXB_1N | O | TXB Negative TMDS differential line driver data output [1] |
| 13 | TXB_1P | O | TXB Positive TMDS differential line driver data output [1] |

| | | | |
|---|---|---|---|
| 14 | TXB_2N | O | TXB Negative TMDS differential line driver data output [2] |
| 15 | TXB_2P | O | TXB Positive TMDS differential line driver data output [2] |
| 16 | TXB_AVDD | Power | Analog 1.2V voltage power supply for TXB Port |
| 17 | TXB_HPD | I | TXB 5V tolerance HPD PAD |
| 18 | TXB_SDA | I/O | TXB 5V tolerance DDC SDA PAD |
| 19 | TXB_SCL | I/O | TXB 5V tolerance DDC SCL PAD |
| 20 | TXB_UTILILY | I | TXB 5V tolerance UTILITY PAD/TXB Audio Return Channel True Input |
| 21 | TXA_SDA | I/O | TXA 5V tolerance DDC SDA PAD |
| 22 | TXA_SCL | I/O | TXA 5V tolerance DDC SCL PAD |
| 23 | TXA_HPD | I | TXA 5V tolerance HPD PAD |
| 24 | TX_PVDD | Power | PLL 1.2V voltage power supply for TX |
| 25 | TXA_AVDD | Power | Analog 1.2V voltage power supply for TXA Port |
| 26 | TVDD | Power | Analog 3.3V voltage power supply |
| 27 | TXA_CN | I/O | TXA Negative TMDS clock output |
| 28 | TXA_CP | I/O | TXA Positive TMDS clock output |
| 29 | TXA_0N | O | TXA Negative TMDS differential line driver data output [0] |
| 30 | TXA_0P | O | TXA Positive TMDS differential line driver data output [0] |
| 31 | TXA_AVDD | Power | Analog 1.2V voltage power supply for TXA Port |
| 32 | TXA_1N | O | TXA Negative TMDS differential line driver data output [1] |
| 33 | TXA_1P | O | TXA Positive TMDS differential line driver data output [1] |
| 34 | TXA_2N | O | TXA Negative TMDS differential line driver data output [2] |
| 35 | TXA_2P | O | TXA Positive TMDS differential line driver data output [2] |
| 36 | TXA_AVDD | Power | Analog 1.2V voltage power supply for TXA Port |
| 37 | DVDD | Power | Digital 1.2V voltage power supply |
| 38 | DVDDIO | Power | Digital IO 3.3V voltage power supply |
| 39 | TXA_AVDD | Power | Analog 1.2V voltage power supply for TXA Port |
| 40 | TXA_AVDD | Power | Analog 1.2V voltage power supply for TXA Port |
| 41 | DVDDIO | Power | Digital IO 3.3V voltage power supply |
| 42 | TXA_AVDD | Power | Analog 1.2V voltage power supply for TXA Port |
| 43 | DVDD | Power | Digital 1.2V voltage power supply |
| 44 | AUD_D0 | I/O | Digital IO PAD for Audio Data0 |
| 45 | AUD_D1 | I/O | Digital IO PAD for Audio Data1 |
| 46 | AUD_D2 | I/O | Digital IO PAD for Audio Data2 |
| 47 | AUD_D3 | I/O | Digital IO PAD for Audio Data3 |
| 48 | AUD_D4 | I/O | Digital IO PAD for Audio Data4 |
| 49 | AUD_D5 | I/O | Digital IO PAD for Audio Data5 |
| 50 | AUD_SCLK | I/O | Digital IO PAD for Audio SCLK |
| 51 | AUD_MCLK | I/O | Digital IO PAD for Audio MCLK |
| 52 | I2C_SDA | I/O | Digital IO PAD for I2C Data |
| 53 | I2C_SCL | I/O | Digital IO PAD for I2C Clock |
| 54 | CSB | I/O | Chip Select Pin |
| 55 | RESETB | I | Reset Pin |
| 56 | INT | O | Interrupt Output Pin |
| 57 | AVMUTE | O | AV-mute Output Pin |
| 58 | DVDD | Power | Digital 1.2V voltage power supply |
| 59 | RX_AVDD | Power | Analog 1.2V voltage power supply for RX port |
| 60 | TVDD | Power | Analog 3.3V voltage power supply |
| 61 | RXA_CN | I | RXA Negative TMDS clock input |
| 62 | RXA_CP | I | RXA Positive TMDS clock input |
| 63 | RXA_0N | I | RXA Negative TMDS differential data input [0] |
| 64 | RXA_0P | I | RXA Negative TMDS differential data input [0] |
| 65 | RX_AVDD | Power | Analog 1.2V voltage power supply for RX port |
| 66 | RXA_1N | I | RXA Negative TMDS differential data input [1] |
| 67 | RXA_1P | I | RXA Negative TMDS differential data input [1] |
| 68 | RXA_2N | I | RXA Negative TMDS differential data input [2] |
| 69 | RXA_2P | I | RXA Negative TMDS differential data input [2] |
| 70 | RX_AVDD | Power | Analog 1.2V voltage power supply for RX port |
| 71 | REXT400 | I/O | External 400ohm resistor to TVDD |
| 72 | CEC | I/O | 5V tolerance CEC PAD |
| 73 | RX_HPD | I/O | RX 5V tolerance HPD PAD |
| 74 | RX_SDA | I/O | RX 5V tolerance DDC SDA PAD |

| | | | |
|---|---|---|---|
| 75 | RX_SCL | I | RX 5V tolerance DDC SCL PAD |
| 76 | RX_5V | Power | RX 5V POWER |

# 3 Electrical Specifications

## 3.1 TMDS Transmitter

### 3.1.1 Transmitter DC and AC Specification

Table 8. TMDS DC and AC Characteristics

| Item | Value |
|---|---|
| Single-Ended High Level Voltage Range: Data Channels 0,1,2 | AVcc-400mV to AVcc+10mV |
| Single-Ended Low Level Voltage Range: Data Channels 0,1,2 | AVcc-1000mV to AVcc-400mV |
| Single-Ended High Level Range: Clock Channel | AVcc-400mV to AVcc+10mV |
| Single-Ended Low Level Voltage Range: Clock Channel | AVcc-1000mV to AVcc-200mV |
| Single-Ended Swing Voltage: Data Channels 0,1,2 | 400mV <=Vswing<=600mV |
| Single-Ended Swing Voltage: Clock Channel | 200mV<=Vswing<=600mV |

### 3.1.2 Transmitter Characteristic

#### 3.1.2.1 TMDS Output Current

- Range: 3mA~18mA, 1mA per step;
- Can be increased by 25% and 50%

## 3.2 Timing Information

### 3.2.1 Power Up and Reset Timing Diagrams

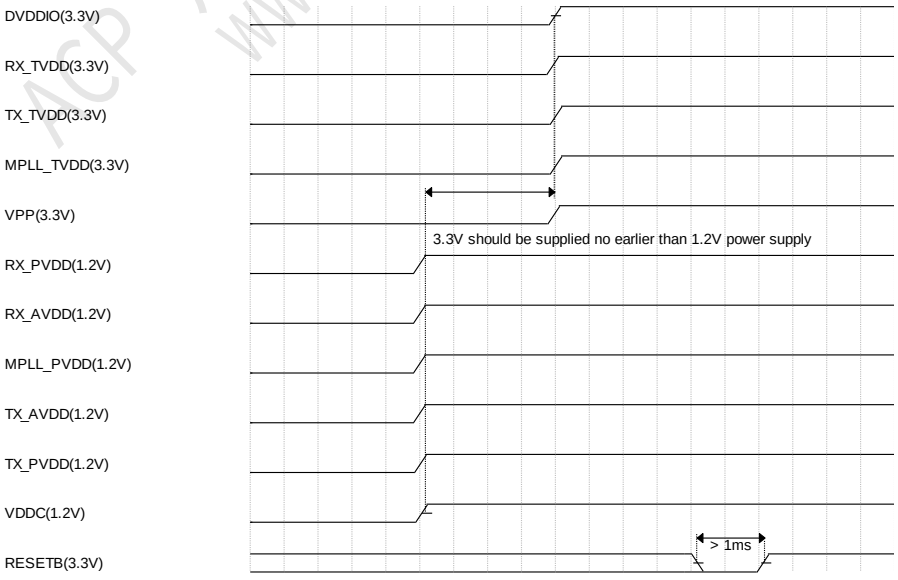



Figure 7. Power Up Sequence

### 3.2.2 I2C Timing Diagrams

The I2C bus used 8-bit page address and 16-bit register address. For every register, 8-bit data will be accessed.

The I2C write timing is shown below.

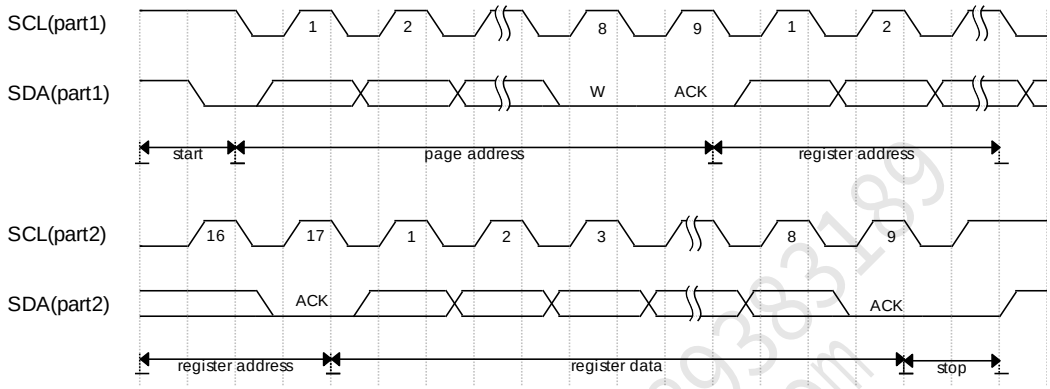



Figure 8. I2C Timing Diagram(Write)

The I2C read timing is shown below.

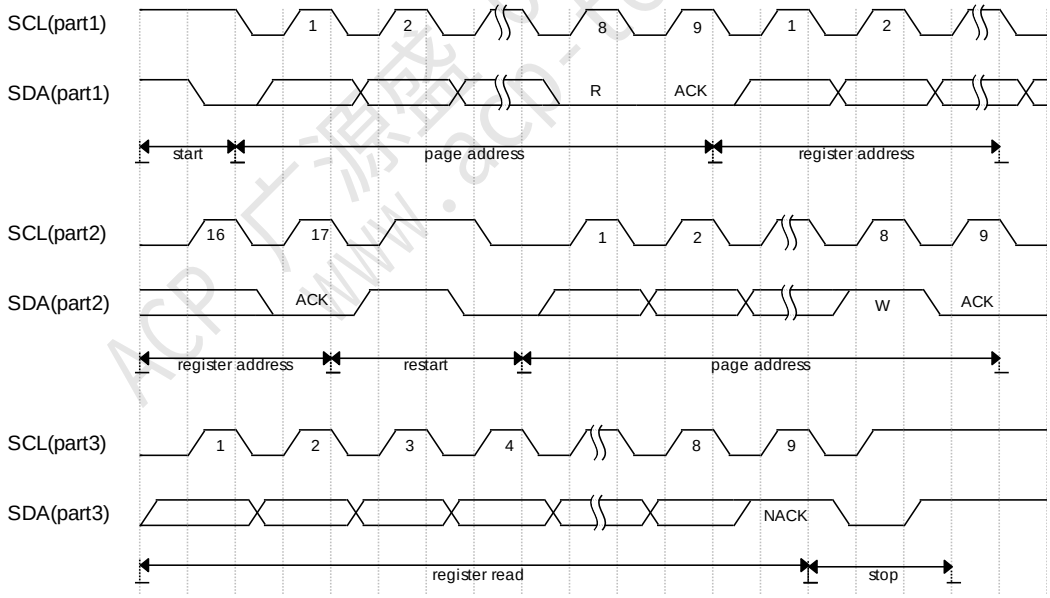



Figure 9. I2C Timing Diagram(Read)

## 3.3 Operating Conditions

### 3.3.1 Temperature Conditions

GSV2001's operation temperature range is -20 ℃ to 85 ℃.
GSV2001's junction termperature can be calculated based on Tj = Tc + θJc *PD.
Use Tc and θJc, PD of GSV2001 max power is 1.35W. θJc is 4.4C/W. Tj can thus be calculated.

### 3.3.2 Power Conditions

GSV2001's power consumption is 1350mW for maximum performance configuration. Typical Case of 1-input, 2-outputs, 4K60 444 with HDCP 2.2 power consumption.

Table 9. 4K60 Power Consumption

| GSV2001 | Power Domain | Current Consumption | Power Consumption |
|---|---|---|---|
| 3.3V | TVDD | 150mA | 0.495W |
| | DVDDIO | <1mA | |
| 1.2V | DVDD | 305mA | 0.366W |
| 1.2V | TX_AVDD | 70mA | 0.462W |
| | RX_AVDD | 215mA | |
| | TX_PVDD | 80mA | |
| | MPLL_PVDD | 20mA | |

### 3.3.3 Audio Pin Conditions

GSV2001's Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

### 3.3.4 I2C Conditions

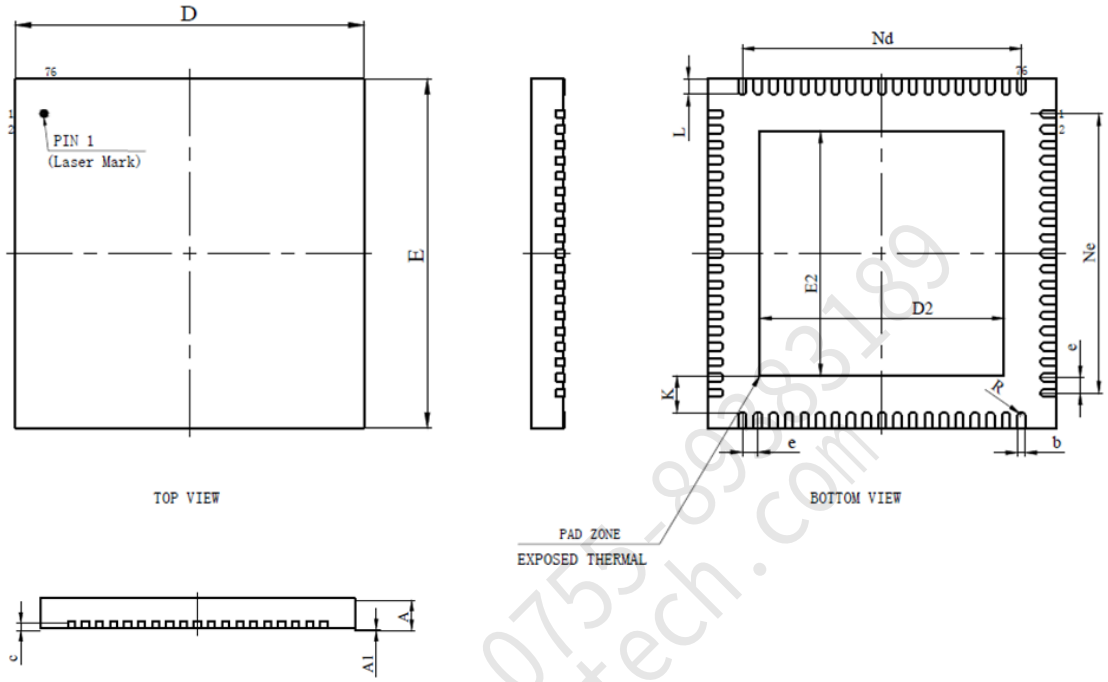
GSV2001's I2C maximum SCL frequency is 400KHz.

### 3.3.5 ESD Conditions

With RCLAMP0524 as external ESD, Rx TMDS and Tx TMDS can both pass 15kV.

# 4 Package Information

The GSV2001 device is packaged in a 76-pin, 9mmx9mm QFN76L package. There is an ePad as the electrical ground of the device. It is critical to solder the entire ePad firmly onto the PCB. A weak connection of the ePad could result in poor performance on higher frequency HDMI video timing.




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | | 0.203REF | |
| D | 8.90 | 9.00 | 9.10 |
| D2 | 6.20 | 6.30 | 6.40 |
| e | | 0.40BSC | |
| Nd | | 7.20BSC | |
| E | 8.90 | 9.00 | 9.10 |
| E2 | 6.20 | 6.30 | 6.40 |
| Ne | | 7.20BSC | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.85 | 0.95 | 1.05 |
| R | 0.075 | -- | -- |

Figure 10. GSV2001 package dimensions

# 5 Ordering Guide

Table 10. Ordering Infomation

| Part Number. | Temperature Range | Package Description | Packing Type |
|---|---|---|---|
| GSV2001 | −20 ℃ to +85 ℃ | QFN76L, 0.4 mm ball pitch, 9 mm x 9 mm outline | Tray |

# 6 Revision History

Table 11. Revision history

| Revision No. | Description | Date |
|---|---|---|
| V0.1 | Draft Initial Version for internal review. | Aug 13, 2018 |
| V0.2 | Characteristics values updated, all supported formats are listed in tables. | Aug 14, 2018 |
| V0.3 | Pin List correction. | Aug 16, 2018 |
| V0.4 | Typo correction. | Aug 17, 2018 |
| V0.5 | Pin List correction again. | Aug 27, 2018 |
| V0.6 | Update HDR support features description. | Nov 5, 2018 |
| V0.8 | Add cascading stages information description. | Jul 11, 2019 |
| V0.9 | Update supported minimum operation temperature. | Jul 31, 2019 |
| V1.0 | Typo correction. | Sep 24, 2019 |
| V1.1 | Add typical soldering profile. | Feb 25, 2021 |
| V2.0 | Reformat the document. | Jun 24, 2021 |

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